REMARKS

The present application was filed on July 30, 2003 with claims 1-14, all of which remain pending. Claims 1, 13 and 14 are the independent claims.

Claims 1-14 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,278,834 (hereinafter "Mazzola").

In this response, Applicants respectfully traverse the §102(b) rejection. Applicants respectfully request reconsideration of the present application in view of the remarks below.

With regard to the §102(b) rejection, Applicants initially note that MPEP §2131 specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicants respectfully traverse the §102(b) rejection on the ground that the Mazzola reference fails to teach or suggest each and every limitation of claims 1-14 as alleged.

Independent claim 1 is directed to a processor comprising controller circuitry and first memory circuitry internal to the processor. The controller circuitry is configurable to determine for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit. The processor is connectable to a second memory circuitry external to the processor. Information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the claimed arrangements are described in the present specification at, for example, page 4, lines 22-28 (describing "an internal memory of the network processor" and "a memory external to the network processor"); page 5, lines 12-19 (with reference to FIG. 1); and page 8, lines 10-14 (with reference to FIG. 4).

The Examiner in formulating the §102(b) rejection argues that the limitations of claim 1 are met by the arrangement shown in FIG. 1 of Mazzola. More specifically, the Examiner argues that memory 14a and 14b are the recited first memory circuitry internal to the processor because memory 14a and memory 14b are used for internal functions of processor 12. See the present Office at page 2, fourth paragraph.

Applicants respectfully disagree. As noted above, claim 1 is directed to a processor comprising first memory circuitry internal to the processor. Applicants respectfully submit that claim 1 therefore requires that the processor itself include the recited first memory circuitry. See, e.g., MPEP 2111.03 (describing the transitional term "comprising" as "synonymous with 'including,' 'containing,' or 'characterized by'").

See also Alliance Gaming Corp. v. Bally Gaming Corp., No. 2006-1342, slip. op. at 6 (Fed. Cir. Sept. 27, 2007) ("In the patent claim context the term 'comprising' is well understood to mean 'including but not limited to.'"); id. at 7 (quoting Robert A. Faber, Landis on Mechanics of Patent Claim Drafting §2:5, 2-15 (5th ed. 2006) ("Other words, less often used, have been given the same meaning in patent claim interpretation as 'comprising': 'including,' 'having,' [and] 'containing'").

Applicants respectfully note that memory 14a and memory 14b refer to areas within memory 14. See, for example, Mazzola at FIG. 1 and at column 3, lines 39-48. Mazzola expressly indicates that memory 14, and hence 14a and 14b, is not contained within processor 12. See, for example, Mazzola at FIG. 1 and at column 3, lines 13-15 ("Each end system node 10 has a processor 12 in communication with a memory 14").

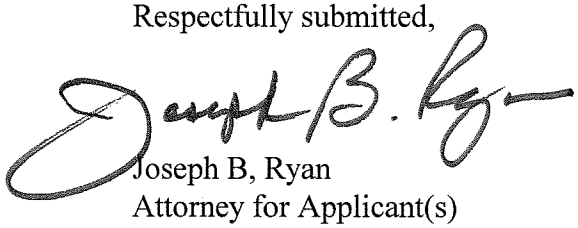
Accordingly, Mazzola fails to teach or suggest the claimed arrangements in which information characterizing a given protocol data unit received by a processor is stored in first memory circuitry internal to the processor if the received protocol data unit is a single-cell protocol data unit, and is stored in second memory circuitry external to the processor if the received protocol data unit is not a single-cell protocol data unit. Rather, by using a memory 14 that is external to processor 12 to store all protocol data units, regardless of whether or not such protocol data units are single-cell units or multi-cell units, Mazzola appears to suffer from the very problems identified by Applicants at page 2, lines 1-13 of the specification.

Independent claims 13 and 14 include limitations similar to those of claim 1, and are believed allowable for reasons similar to those described above with reference to claim 1.

Dependent claims 2-12 are believed allowable for at least the reasons identified above with regard to claim 1. One or more of these claims are also believed to define separately-patentable subject matter over the cited art.

In view of the above, Applicants believe that claims 1-14 are in condition for allowance, and respectfully request withdrawal of the §102(b) rejection.

Respectfully submitted,



Date: November 30, 2007

Joseph B, Ryan
Attorney for Applicant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517